

# 14 Pin DIL 10 Tap TTL Compatible Active Delay Lines MIL 883

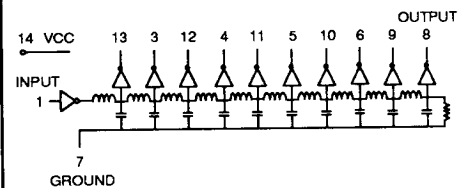
TAP DELAYS ±5% or ±2 nS	TOTAL DELAYS ±5% or ±2 nS	PART NUMBER	TAP DELAYS ±5% or ±2 nS	TOTAL DELAYS ±5% or ±2 nS	PART NUMBER
5	50	EP9749-50	44	440	EP9749-440
6	60	EP9749-60	45	450	EP9749-450
7.5	75	EP9749-75	47	470	EP9749-470
10	100	EP9749-100	50	500	EP9749-500
12.5	125	EP9749-125	55	550	EP9749-550
15	150	EP9749-150	60	600	EP9749-600
17.5	175	EP9749-175	65	650	EP9749-650
20	200	EP9749-200	70	700	EP9749-700
22.5	225	EP9749-225	75	750	EP9749-750
25	250	EP9749-250	80	800	EP9749-800
30	300	EP9749-300	85	850	EP9749-850
35	350	EP9749-350	90	900	EP9749-900
40	400	EP9749-400	95	950	EP9749-950
42	420	EP9749-420	100	1000	EP9749-1000

Delay times referenced from input to leading edges

All units are supplied with ceramic IC's that have been screened to MIL-STD-883

DC Electrical Characteristics		Test Conditions	Min	Max	Unit
$V_{OH}$	High-Level Output Voltage	$V_{CC} = \text{min. } V_{IL} = \text{max. } I_{OH} = \text{max}$	2.7		V
$V_{OL}$	Low-Level Output Voltage	$V_{CC} = \text{min. } V_{IH} = \text{min. } I_{OL} = \text{max}$		0.5	V
$V_{IK}$	Input Clamp Voltage	$V_{CC} = \text{min. } I_I = I_{IK}$		-1.2V	V
$I_{IH}$	High-Level Input Current	$V_{CC} = \text{max. } V_{IN} = 2.7V$		50	$\mu A$
		$V_{CC} = \text{max. } V_{IN} = 5.25V$		1.0	mA
$I_{IL}$	Low-Level Input Current	$V_{CC} = \text{max. } V_{IN} = 0.5V$		-2	mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{max. } V_{OUT} = 0.$ (One output at a time)	-40	-100	mA
$I_{CCH}$	High-Level Supply Current	$V_{CC} = \text{max. } V_{IN} = \text{OPEN}$		150	mA
$I_{CCL}$	Low-Level Supply Current	$V_{CC} = \text{max. } V_{IN} = 0$		150	mA
$T_{RO}$	Output Rise Time	$T_d \leq 500 \text{ nS (0.75 to 2.4 Volts)}$ $T_d > 500 \text{ nS}$		4	nS
				5	nS
$N_H$	Fanout High-Level Output	$V_{CC} = \text{max. } V_{OH} = 2.7V$		20 TTL LOAD	
$N_L$	Fanout Low-Level Output	$V_{CC} = \text{max. } V_{OL} = 0.5V$		10 TTL LOAD	

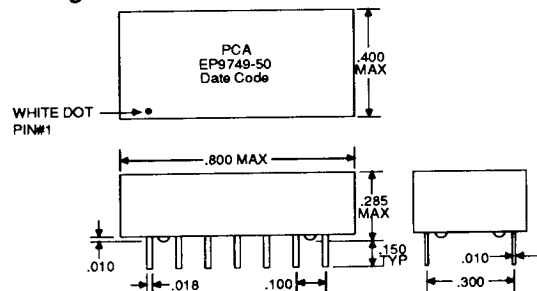
## Schematic



Recommended Operating Conditions		Min	Max	Unit
$V_{CC}$	Supply Voltage	4.5	5.5	V
$V_{IH}$	High-Level Input Voltage	2.0		V
$V_{IL}$	Low-Level Input Voltage		0.8	V
$I_{IK}$	Input Clamp Current		-18	mA
$I_{OH}$	High-Level Output Current		-1.0	mA
$I_{OL}$	Low-Level Output Current		20	mA
$PW^*$	Pulse Width of Total Delay	40		%
$d^*$	Duty Cycle		40	%
$T_A$	Operating Free-Air Temperature	-55	+125	$^{\circ}C$

\*These two values are inter-dependent.

## Package Dimensions



Input Pulse Test Conditions @ 25 $^{\circ}C$			Unit
$E_{IN}$	Pulse Input Voltage	3.2	Volts
$PW$	Pulse Width % of Total Delay	110	%
$T_{RI}$	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
$PRR$	Pulse Repetition Rate @ $T_d \leq 200 \text{ nS}$	1.0	MHz
	Pulse Repetition Rate @ $T_d > 200 \text{ nS}$	100	KHz
$V_{CC}$	Supply Voltage	5.0	Volts

16799 SCHOENBORN ST.  
SEPULVEDA, CA 91343  
TEL: (818) 892-0761  
FAX: (818) 894-5791  
TWX: (910) 496-1525